Performance challenges in audio converter design

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Objective

• The usual design methodology for converter sub-systems is to…
  Choose a data converter which suits your needs
  Implement the design based on the manufacturer’s application note
• But often the design underperforms the potential of the chip…
  Either all the time, or in certain situations
  This talk is about the main causes for this, IMHO
  But first I should explain…
• Why data converters are sorted
  Modern flagship off-the-shelf data converters can exceed 130dB DR
  and -110dB THD+n; most converter sub-systems can’t
  So it’s hard to justify spending time designing a data converter
  OK, maybe not the decimation and interpolation filters
Typical ADC

Performance-critical parts

- Vref
- PLL
- Input conditioning
- Decimation filter
- Digital parts
- DSP functions
- DIT
- PSU
- Sync

Prism Sound
Converter clocking issues

- The conversion clock is critical to audio performance
  Any irregularity results in sampling jitter which causes phase modulation of the converted signal
- The conversion clock usually needs to be recovered using a PLL
  Most equipment cannot be clock master all the time
- PLL design can embody some unpalatable tradeoffs; we need to achieve:
  - High jitter rejection down to low frequencies
  - Low intrinsic jitter over a wide bandwidth
  - Wide (enough) lock range
  - Fast lock-up
  - Ability to accommodate low reference frequencies (video, timestamps etc.)
- But...
  - Wide-range VCOs have lots of phase-noise…
  - …but low phase-noise VCOs have narrow pull range
  - PLL needs to be a big flywheel for good jitter rejection…
  - …but a small flywheel to control VCO phase noise
Analogue PLL operation

- **Phase comparator**
- **Loop filter**
- **VCO**
- **Ref** / 2^n
- **2^n*Ref**
- **Converter clock**

Jitter rejection

Output phase noise (intrinsic jitter) spectrum

High corner frequency

Low corner frequency
Some analogue PLL solutions

- **Common, e.g. using DIR in DAC**
  - Poor intrinsic jitter (RC multivibrator)
  - Poor jitter rejection (high corner frequency)
  - Good lock range
  - Low cost

- **Often found in better equipment**
  - Good intrinsic jitter (hiQ quartz VCXO)
  - Good jitter rejection (low corner frequency)
  - Possibly inadequate lock range (hiQ quartz)
  - High cost (two or more VCXOs)

- **Good overall analogue solution**
  - Good intrinsic jitter (LF hiQ and HF loQ)
  - Good jitter rejection (PLL1)
  - Good lock range (LGS: lower Q than quartz)
  - Moderate cost (only one VCXO)
Example of a hybrid PLL

From Cirrus CS2000 datasheet
Power supply issues

• Switching PSUs have many advantages over linear:
  Linear PSUs are large, heavy, inefficient (hot) and expensive
  Switching PSUs aren’t, but…

• They are often feared by high-end audio designers who perceive them as:
  An unmanageable source of interference into the analogue audio parts
  An EMC approval headache
  A reliability risk

• Yet…
  They can be tamed
  In DC-powered cases, they may be a necessity
Drawbacks of a basic SMPS

Flyback converter is a popular choice…

From ST application note AN1326
Resonant SMPS topologies

- **Wouldn’t it be nice if we had 500kHz mains?**
  Resonant SMPS approximates a sine wave through the transformer, by adding a resonant tank circuit in the primary, with zero-current/voltage switching.
  It’s more complex and expensive than the simple flyback SMPS, and may be difficult to operate in off-line universal-input mode.
  But we only really need to achieve resonant operation at the switching points.

- **Quasi-resonant SMPS**
  A simple adaptation of a basic flyback converter, which uses resonance at the switching points to reduce switching noise and losses.

- **Difficulty in selecting appropriate SMPS topology for audio**
  Manufacturers’ selection guides recommend simple topologies for low-power applications.
  But for audio, interference can be reduced by designing low-power versions of higher-power topologies.
Quasi-resonant SMPS

From NXP TEA1507 application note
EMI improvement

Flyback SMPS conducted EMI

Quasi-resonant SMPS conducted EMI

From ST application note AN1326
Other SMPS considerations

• Cross-regulation
  Critical rails may benefit from linear post-regulation

• Power-factor-correction (PFC)
  Reduces power-line distortion
  Can be useful in guaranteeing constant DC at SMPS input for improved resonant and quasi-resonant performance

• Beware recent efficiency legislation/guidelines
  EU Ecodesign Directive, US EnergyStar
  Typically >80% efficiency for <20W units
  And <0.5W when units are in ‘standby’
Analogue signal path issues

• Opamp stages (for that is what we shall use…)
  Understand opamp circuit noise models
  Choose the gain structure so as to maximize the signal
  Choose the right topologies, e.g. inverting stages usually cause less distortion than non-inverting
  Consider a balanced signal path throughout
  Think about bandwidth
  Choose the best opamp ‘on paper’ for each job – then try some others
  Remember: there is no ‘best audio opamp’

• Converter buffers
  ΣΔ ADC inputs often have non-linear characteristics and all alias HF, requiring careful ADC buffer design
  Current output DACs require careful IVC design
Analogue signal path issues

- **Passive components**
  - Resistor types: metal film or thin film (thick film ‘chip’ resistors are nasty)
  - Capacitor types: C0G/NP0 ceramic or low-loss plastic e.g. polystyrene

- **Physical**
  - Ground planes, small SMT components, laying down where possible
  - Tight channel strip layout, output/ground nodes outward, input nodes inward, consider dual opamp packages
  - Consider galvanic isolation between analogue and digital domains
  - Lots of test points, especially on the prototype
Look after the reference voltage…

• The reference voltage is very important
  The input to the converter is multiplied by its reference voltage (or current) to produce the output, so the reference is just as critical as the analogue path
  Reference care is your responsibility - keep connections very short
  Pay attention to reference voltage decoupling capacitors
  Consider driving reference voltage pins from a quiet, well-regulated external source (not the power rail!)
  Pay attention to reference current IVC resistors

• A tip:
  If you have an elusive performance problem and the analogue signal path looks fine: don’t forget the reference
  If it looks like modulation (sidebands or a noise skirt around the signal frequency): if it gets worse with increasing signal frequency, it’s jitter; if it doesn’t, it’s probably a reference voltage problem
Digital path issues

• Digital processing (including ‘accidental’ processing)
  Make sure that any bundled DSP functions maintain sufficient precision not to let the analogue part down
  Make sure that WLR schemes (dither, noise shaping etc.) pass on pre-WLR linearity below the WLR noise floor
  For computer interfaces, remember the driver and the parts of the OS that you thought weren’t involved – it’s vital to have test gear to generate/analyze in the ‘computer domain’

• Interference
  Modern converter sub-systems contain many hostile asynchronous digital parts; despite lower voltages and smaller packages, modern chips have fast edge times which are hostile irrespective of operating frequency
  Try to merge functionality into fewer devices, e.g. FPGAs
  Observe good EMC design practices
System considerations

• Major decisions to make at the outset, although probably dictated by project requirements:
  Power source: DC-powered (wart or ‘computer bus’), or line-powered (linear or SMPS supply?)
  Habitat: own housing, or cohabiting with digital parts, or worse in host computer? Do we need/can we afford screening cans?
  Manufacturing technology: SMT or THP, or mixed? Number of PCB layers available may affect plane topology
  Isolation: can we galvanically isolate analogue and digital grounds using optical or magnetic isolators?
  EMC, efficiency: what statutory/voluntary directives will apply?
Assessment

• Measurement vs listening
  It’s better to debug and refine the design through objective measurement before subjective evaluation

• Equipment
  An audio analyzer which can generate/analyze in the analogue and digital domains (including the ‘computer domain’) is vital
  An RF spectrum analyzer is useful for wideband inspection, especially in SMPS and computer-based designs; needed for EMC pre-compliance in any case

• I like to…
  Set up the audio analyzer to be able to switch conveniently between the important measurements
  Display a high-resolution FFT all the time – it’s very handy when tinkering
### Summary of converter transparency parameters

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